# IMPROVED BALL GRID ARRAY PACKAGE AND PROCESS FOR MANUFACTURING SAME

## CROSS REFERENCE TO RELATED APPLICATION

**[0001]** This is a continuation-in-part of co-pending United States patent application No. 10/323,657 entitled, Process For Manufacturing Ball Grid Array Package, filed December 20, 2002, which is a continuation-in-part of United States patent application serial no. 10/197,832 entitled Improved Ball Grid Array Package, filed July 19, 2002. Now US. Pat. No. 6,800,948

## FIELD OF THE INVENTION

**[0002]** The present invention relates in general to integrated circuit packaging, and in particular to an improved ball grid array package with enhanced thermal characteristics and a unique method of manufacturing the ball grid array package.

## BACKGROUND OF THE INVENTION

**[0003]** High performance integrated circuit (IC) packages are well known in the art. Improvements in IC packages are driven by industry demands for increased thermal and electrical performance and decreased size and cost of manufacture.

**[0004]** In general, array packaging such as Plastic Ball Grid Array (PBGA) packages provide a high density of interconnects relative to the surface area of the package. However, typical PBGA packages include a convoluted signal path, giving rise to high impedance and an inefficient thermal path which results in low thermal dissipation performance. With increasing package density, the spreading of heat generated by the package is increasingly important.

**[0005]** Reference is made to Figure 1, which shows an elevation view of a conventional PBGA package indicated generally by the numeral 20. The PBGA package 20 includes a substrate 22 and a semiconductor die 24 attached to the substrate 22 by a die adhesive. Gold wire bonds 26 electrically connect the die 24 to metal traces on the substrate 22. The wire bonds 26 and die 24 are encapsulated in a molding compound 28. Solder balls 30 are disposed on the bottom surface of the substrate 22 for signal transfer. Because of the absence of a thermal path away from the semiconductor die 24, thermal dissipation in this package is poor.